REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1, 3-34, and 36-69 remain pending. Claims 1, 3-34, and 36-69 have been rejected.

Claims 1 and 34 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

Claims 1, 5-7, 11-14, 17-20, 23-30, 32-34, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,446,198, to Sazegari ("Sazegari").

Applicants have amended claim 1 to include receiving a string of bits having a first plurality of segments; receiving a plurality of data elements including a control information specifying a location and a length of a second plurality of segments in the string of bits; and generating a plurality of indices for one or more look-up tables that includes selecting the second plurality of segments from the first plurality of segments based on the control information.

It is respectfully submitted that such amendments are supported by the specification, drawings, and claims as originally filed. The specification discloses, in part, the following:

> **Figure 51** illustrates a block diagram representation of a circuit for the execution of a method to perform variable length decoding according to one embodiment of the present invention. A bit stream is stored in entry 7101 in a vector register file. The bit stream contains a number of code words to be decoded. Bit pointer 7152, table offset 7151, escape format 7153, and fence bits 7154 are stored in other entries of the vector register file. After the execution unit receives control information for the instruction dispatcher, bit selectors 7103 select a number of bit segments from bit stream 7101 to generate indices 7121, 7122, ..., 7129 for look-up tables 7109 using local control information 7111, 7112, ..., 7119. Bit pointer 7152 indicates the position of the starting bit of the current code word in the bit stream. Local control information 7111, 7112, ..., 7119 are stored in an entry of

the vector register file. Each of the local control information indicates a location and a length of the bit segment to be selected from the bit stream to construct the index. Table offset 7151 is combined with the bit segments selected by bit selectors 7103 to generate the indices. The details of one embodiment of the bit selector are illustrated in **Figure 54**, and will be described in the following paragraphs.

(the specification, paragraph [00267], Figure 51)(emphasis added)

Therefore, applicants respectfully submit that receiving a string of bits having a first plurality of segments; receiving a plurality of data elements including a control information specifying a location and a length of a second plurality of segments in the string of bits; and generating a plurality of indices for one or more look-up tables that includes selecting the second plurality of segments from the first plurality of segments based on the control information, as recited in amended claim 1, is supported by the specification.

Sazegari discloses the permute mask 26. More specifically, Sazegari discloses the following:

> …logically dividing a large table into a number of smaller tables that can be uniquely indexed with a permute instruction. For instance, a 256-byte table can be logically divided into eight 32-byte tables. Each smaller table consists of two data vectors, which constitute the operands for the permute instruction. Only a limited number of bits in the permute instruction vector are required to index into the table during execution, e.g. five bits in the case of a 32-byte table."

(Sazegari, col. 2, lines 17-26)(emphasis added)

In particular, Sazegari discloses the following:

> For table lookup operations, the permute instruction can be used to perform 16 simultaneous lookup operations on a 32-byte entry table. FIG. 4 illustrates such a table 34, which consists of two 16-byte vectors, data1 and data2. Each vector can be stored in one register of the CPU. The permute instruction can be used to simultaneously read 16 values from these two vectors, in accordance with index values in a register 36, and store the 16 output results in sequential order in another register 38.

(Sazegari, col. 4, lines 24-32)(emphasis added)

Thus, Sazegari merely discloses using index values in a register file to read values. In contrast, amended claim 1 refers to selecting a second plurality of segments from a first plurality of segments based on the control information indicating a location and length of the second plurality of segments to generate a plurality of indices for one or more look-up table.

Accordingly, Sazegari fails to disclose receiving a string of bits having a first plurality of segments; receiving a plurality of data elements including a control information specifying a location and a length of a second plurality of segments in the string of bits; and generating a plurality of indices for one or more look-up tables that includes selecting the second plurality of segments from the first plurality of segments based on the control information, as recited in amended claim 1.

Because Sazegari fails to disclose all limitations of amended claim 1, applicants respectfully submit that claim 1, as amended, is not anticipated by Sazegari under 35 U.S.C. § 102(e).

For at least the similar reasons, applicants respectfully submit that claims 5-7, 11-14, 17-20, 23-30, 32-35, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 are not anticipated by Sazegari under 35 U.S.C. § 102(e).

Claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64, and 69 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari in view of the Examiner's taking of Official Notice.

As set forth above, Sazegari fails to disclose, teach, or suggest selecting a second plurality of segments from a first plurality of segments based on the control information indicating a location and length of the second plurality of segments to generate a plurality of indices for one or more look-up tables, as recited in amended claim 1.

Given that claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64 and 69 contain the limitations that are similar to those limitations discussed with respect to amended claim 1, applicants respectfully submit that claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64 and 69 are not obvious under 35 U.S.C. § 103(a) over Sazegari.

The Examiner has rejected claim 67 under 35 U.S.C. § 103(a) as being unpatentable over Sazegari in view of U.S. Patent No. 5,526,501 to Shams ("Shams").

It is respectfully submitted that Shams also fails to disclose, teach, or suggest selecting a second plurality of segments from a first plurality of segments based on the control information indicating a location and length of the second plurality of segments to generate a plurality of indices for one or more look-up tables, as recited in amended claim 34.

Furthermore, even if the addressing scheme of Shams were incorporated into a vectorized table lookup of Sazegari, such a combination would still lack selecting a second plurality of segments from a first plurality of segments based on the control information indicating a location and length of the second plurality of segments to generate a plurality of indices for one or more look-up tables, as recited in amended claim 1.

Given that claim 67 depends from amended claim 1, and adds additional limitations, applicants respectfully submit that claim 67 is not obvious under 35 U.S.C. § 103(a) over Sazegari in view of Shams.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 022666 for any fee deficiency that may be due.

Respectfully submitted,

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